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Description

METHOD TO SELECTIVELY CORRECT CRITICAL DIMENSION ERRORS IN THE SEMICONDUCTOR INDUSTRY

BACKGROUND ART

[0001] Background of the Invention

[0002] 1. Technical Field

[0003] The present invention relates to a method for correcting critical dimension errors during a semiconductor device or semiconductor mask manufacturing process.

[0004] 2. Related Art

[0005] During a manufacturing process, electrical components within an electrical circuit may not be produced within design specifications. Electrical components within an electrical circuit that are not fabricated to the design specifications may cause the electrical circuit to malfunction or operate incorrectly. Therefore there exists a need to produce electrical components during a manufacturing process that meet design specifications for both physical and electrical characteristics.

[0006] Summary of the Invention

[0007] The present invention provides a method, comprising:

[0008] providing a first semiconductor device;

[0009] analyzing the first semiconductor device to determine at least one critical dimension error within the first semiconductor device;

[0010] determining from said at least one critical dimension error, a dose of electron beam exposure to correct the at least one critical dimension error during a subsequent process to form a second semiconductor device, said subsequent process comprising;

[0011] providing a semiconductor structure, wherein the semiconductor structure comprises a photoresist layer on a semiconductor substrate;

[0012] forming a plurality features in the photoresist layer, wherein at least one feature of the plurality of features comprises the at least one critical dimension error;

[0013] correcting the at least one critical dimension error by exposing the at least one feature comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure.

[0014] The present invention provides a method, comprising:

[0015] providing a mask and a semiconductor structure, wherein the semiconductor structure comprises a photoresist layer on a semiconductor substrate;

[0016] measuring on the mask, a plurality of critical dimensions within a pattern on the mask to determine at least one critical dimension error within said pattern;

[0017] propagating radiation through the mask to expose the photoresist layer to form a plurality of features in the photoresist layer, wherein at least one feature of the plurality of features comprises the at least one critical dimension error from the pattern on the mask;

[0018] determining from said at least one critical dimension error from the pattern on the mask, a dose of electron beam exposure that will be used to correct the at least one critical dimension error for the at least one feature comprising the at least one critical dimension error; and

[0019] correcting the critical dimension error by exposing the at least one feature comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure that corrects the critical dimension error of the at least one feature.

[0020] The present invention provides a method, comprising:
providing a semiconductor structure, wherein the
semiconductor structure comprises a photoresist layer on a semiconductor substrate;

[0021] forming a plurality of features in the photoresist layer;

[0022] measuring a plurality of critical dimensions of the plurality of features to determine at least one critical dimension error for at least one feature of the plurality of features;

[0023] determining from said at least one critical dimension error, a dose of electron beam exposure to correct the at least one critical dimension error for the at least one feature of the plurality of features;

[0024] correcting the at least one critical dimension error by exposing the at least one feature comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure that corrects the critical dimension error of the at least one feature.

[0025] The present invention provides a method, comprising:

[0026] providing a mask photoresist layer;

[0027] forming a plurality of features in the mask photoresist layer;

[0028] measuring a plurality of critical dimensions of the plurality of features in the mask photoresist layer to determine at least one critical dimension error for at least one

feature of the plurality of features;

[0029] determining from said at least one critical dimension error, a dose of electron beam exposure that will be used to correct the at least one critical dimension error for the at least one feature comprising the at least one critical dimension error; and

[0030] correcting the critical dimension error by exposing the at least one feature comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure that corrects the critical dimension error of the at least one feature.

[0031] The present invention advantageously provides a method to produce electrical components during a manufacturing process that are design specifications for both physical and electrical characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] FIG. 1 illustrates a flowchart describing an algorithm for determining and correcting a critical dimension (CD) error(s) for a feature(s) produced on a semiconductor substrate, in accordance with embodiments of the present invention.

[0033] FIG. 2A illustrates a system comprising a device for emitting radiation through a photomask onto a photoresist layer, in accordance with embodiments of the present invention.

[0034] FIG. 2B illustrates the photoresist layer of FIG. 2A that has undergone a photochemical change has become insoluble due to the diverted radiation of FIG. 2A in accordance with embodiments of the present invention.

[0035] FIG. 3A illustrates a system comprising a device for emitting an electron beam onto a feature to correct a critical dimension error, in accordance with embodiments of the present invention.

[0036] FIG. 3B illustrates a reduced dimension of a feature from FIG. 3A, in accordance with embodiments of the present invention

[0037] FIG. 4A is a flowchart depicting an algorithm for a first photomask based method for correcting a critical dimension error, in accordance with embodiments of the present invention.

[0038] FIG. 4B is a flowchart depicting an algorithm for a second photomask based method for correcting a critical dimension error, in accordance with embodiments of the present invention.

[0039] FIG. 5 is a flowchart depicting an algorithm for a photoresist based method for correcting a critical dimension error, in accordance with embodiments of the present invention.

[0040] FIG. 6 is a flowchart depicting an algorithm for a final semiconductor device based method for correcting a critical dimension error, in accordance with embodiments of the present invention.

[0041] FIG. 7 illustrates a graph for providing a relationship between a plurality critical dimension size changes for a feature(s) and a plurality electron beam exposures to the feature, in accordance with embodiments of the present invention.

DISCLOSURE OF INVENTION

[0042] FIG. 1 illustrates a flowchart describing an algorithm for determining and correcting a critical dimension (CD) error(s) for a feature(s) within a photoresist layer, wherein said feature(s) is to be subsequently transferred to a semiconductor substrate during a photolithography process, in accordance with embodiments of the present invention. Thus, a feature(s) will ultimately define a corresponding structure within the semiconductor substrate. The term “critical dimension error ” (CD error) is defined herein as an incorrect dimension for the feature(s). The CD error may be

caused during a photolithography process by, inter alia, an incorrect pattern or image within a mask, an error during a pattern transfer from the mask to the photoresist, an incorrect original design, etc. The CD error(s) is corrected during a semiconductor device manufacturing process at a photoresist level without building a new mask. Although the following description is described with reference to photolithography using radiation (e.g., laser 6A and 6B) and a mask, note that any lithography method known to a person of ordinary skill in the art may be used including, inter alia, a maskless lithography method, a direct write lithography method, etc. During the during a photolithography process (i.e., using radiation), a photomask (see mask 9 in FIG. 2A) is used to produce a plurality of features (e.g., feature 15B in FIG. 2B) within a semiconductor wafer (see semiconductor wafer 19 in FIG. 2B). Radiation is provided through the mask to project a patterned image on a photoresist layer that will define the plurality of features within the photoresist layer that remains after a subsequent process (e.g., chemical etch) that removes soluble portions of the photoresist layer. In turn, the plurality of features in the photoresist layer are utilized to define a plurality of structures, inter alia, doping regions, deposition regions, etching regions, isolation regions, transistor gates, and other device structures and elements (e.g., electrical components) within the semiconductor substrate. Additionally, the plurality of features in the photoresist layer may also define conductive lines or conductive pads associated with metal layers within the semiconductor substrate. During the above described process, the CD error(s) for the feature(s) within the layer of photoresist material on the semiconductor substrate may be caused by, inter alia, an incorrect pattern or image on a mask, an error during a pattern transfer from the mask to the photoresist, lens aberration during the image projection, an incorrect original design, etc. The CD error is corrected at a photoresist layer level as described below by FIG. 1.

[0043]

In step 2 of FIG. 1, a mask comprising a specific design for producing features to be

transferred to a layer of photoresist material on a semiconductor substrate is built or provided. In step 3 CD error(s) are determined. Methods for determining the CD error(s) are described with reference to FIGS. 4, 5, and 6. In step 5, the CD error(s) is corrected at a photoresist level. A system for correcting the CD error(s) is described with reference to FIGS. 2A, 2B, 3A, and 3B.

[0044] FIG. 2A illustrates a system 1 comprising a device 10 for emitting radiation 6A and 6B through a photomask 9 on to a photoresist layer 15A disposed on a substrate 18, in accordance with embodiments of the present invention. The photoresist layer 18 is assumed to use a positive photoresist but may alternatively comprise a negative photoresist if the inverse pattern is used in the mask 9 of FIGS. 2A and 2B. A semiconductor wafer 19 comprises the photoresist layer 15A and the substrate 18. The substrate 18 may comprise a semiconductor substrate. The substrate 18 may comprise a semiconductor substrate and an insulating layer. The device 10 may be any radiation emitting device known to a person of ordinary skill in the art that emits radiation at a wavelength such that the radiation photochemically reacts with the resist material of the photoresist layer 9. The radiation 6A propagating through the photomask 9 is selectively transmitted (i.e., becoming radiation 6B) to a specified area 17 on the photoresistst layer 15A as defined by the patterned image on the photomask 9. The specified area 17 on the photoresist layer 15A that the radiation 6B makes contact with will undergo a photochemical change such that specified area 17 on the photoresist layer 15A becomes soluble or insoluble if a negative photoresist is used.

[0045] FIG. 2B illustrates that the specified area 17 on the photoresist layer 15A from FIG. 2A has undergone a photochemical change and has been removed such as by chemical developing, in accordance with embodiments of the present invention. Thus, all that remains of the photoresist layer 15A from FIG. 1 is a feature 15B in FIG. 2B. The feature 15B will be utilized to define a structure, inter alia, doping

regions, deposition regions, etching regions, isolation regions, transistor gates, other device structures and elements (e.g., electrical components), conductive lines or conductive pads associated with metal layers, etc within the semiconductor wafer 19. The feature 15B is determined to comprise a critical a dimension error (determining CD errors is described with reference to FIGS. 4,5, and 6). A method to correct the CD error (at the photoresist level) is described with reference to FIGS. 3A and 3B.

[0046]

FIG. 3A illustrates a system 6 comprising a device 4 for emitting an electron beam onto the feature 15B to correct a CD error, in accordance with embodiments of the present invention. The device 4 may be, inter alia, a scanning electron microscope (SEM), an electron beam direct write lithography tool, or large spot electron beam emitter, etc. The electron beam 22 is a low energy electron beam (e.g., electron beam in a range of about 250 electron volts (eV) to about 10000 eV). The electron beam 22 is emitted in a specified dose dependent upon a size of the CD error (i.e., how much correction is needed). The feature may be exposed to multiple emissions of the electron beam 22, each emission of the electron beam being at a specific power level for a specific amount of time (i.e., eV/unit of time). The dose of electron beam exposure is dependent upon a size of the CD error, and the physical properties of the feature with the CD error. For example, FIG. 7 illustrates (as described supra) a graph showing 3 second exposures to a 500 eV electron beam, 10 times. The feature 15B comprises a dimension D1 (e.g., length) that has been determined to be an incorrect dimension (i.e., a CD error). In response to the CD error, the electron beam 22 is directed on the feature 15B to reduce (i.e., shrink) the dimension D1 of the feature 15B to a smaller dimension D2 to become feature 15C in FIG. 3B. The dimension D1 of the feature 15B is reduced to the smaller dimension D2 of a feature 15C due to a chemical breakdown, and out gassing of the photoresist material and any entrapped solvent that occurs when the electron

beam 22 makes contact with the feature 15B. The difference between the dimension D1 and the dimension D2 accounts for the CD error and therefore the feature 15C comprising the dimension D2 does not comprise the CD error.

[0047] FIG. 3B illustrates the reduced dimension D2 of a feature 15C, in accordance with embodiments of the present invention. The dimension D2 of a feature 15C has been reduced from the D1 of the feature 15B in FIG. 3A as described with reference to FIG. 3A.

[0048] FIG. 4A is a flowchart depicting an algorithm 22 for a first photomask based method for correcting a CD error at a photoresist level, in accordance with embodiments of the present invention. The algorithm 22 is described with reference to FIGS, 2A, 2B, 2C, and 2D. In step 24, a photomask (e.g., photomask 9 in FIG. 2A) is designed and built for a photolithography process to produce a semiconductor device(s). In step 27, a pattern or image on the photomask is measured to determine if there are any CD errors that will produce a CD error in a feature (e.g., feature15B in FIG. 2B) during the photolithography process. Measuring techniques may include, inter alia, using a SEM, etc. If there is not an error(s) found in the photomask in step 27, then in step 28 the photomask may be used to produce a semiconductor device(s). If there is a CD error found in the photomask in step 27, then in step 30 the CD error is analyzed to determine a dose of electron beam exposure that may be used to correct the CD error in a subsequent step. A method for determining the dose of electron beam exposure is described with reference to FIG. 7 as described, infra. In step 34, radiation (e.g., radiation 6A and 6B in FIG. 2A) is propagated through the photomask comprising the CD error thereby resulting in a feature(s) (e.g., feature 15B in FIG. 2B) comprising the CD error. In step 36, the feature(s) is exposed to the dose of electron beam exposure, thereby shrinking the feature size, and ultimately correcting the CD error (e.g., feature 15C in FIG. 3B). In step 42 a semiconductor device manufacturing process is completed thereby producing a semiconductor

device(s) (e.g., a semiconductor chip) without a CD error(s).

[0049] FIG. 4B is a flowchart depicting an algorithm 23 for a second photomask based method for correcting a CD error at a mask 9 photoresist level, in accordance with embodiments of the present invention. The algorithm 23 occurs during step 2 of FIG. 1 as a photomask is built. In step 114, a pattern (i.e., a feature) is formed in the photomask photoresist layer (e.g., photomask 9 in FIG. 2A). In step 115, a pattern or image formed the photomask is measured to determine if there are any CD errors in the photomask photoresist layer that will produce a CD error in a feature (e.g., feature15B in FIG. 2B) during a photolithography process. Measuring techniques may include, inter alia, using a SEM, etc. If there is not an error(s) found in the photomask photoresist layer in step 115, then in step 116 the processing is continued to produce a final photomask. The final photomask may be used to produce a semiconductor device(s). If there is a CD error found in the photomask photoresist layer in step 115, then in step 117 the CD error is analyzed to determine a dose of electron beam exposure that may be used to correct the CD error (i.e., in the photomask photoresist layer) in a subsequent step. A method for determining the dose of electron beam exposure is described with reference to FIG. 7 as described, infra. In step 119, the photomask photoresist layer is selectively exposed to the dose of electron beam exposure, thereby shrinking a feature(s) size in the photomask photoresist layer, and ultimately correcting the CD error. In step 124, processing is continued to produce a final photomask without a CD error(s).

[0050] FIG. 5 is a flowchart depicting an algorithm 47 for a photoresist based method for correcting a CD error at a photoresist level, in accordance with embodiments of the present invention. The algorithm 47 is described with reference to FIGS. 2A, 2B, 2C, and 2D. In step 49, a photomask (e.g., photomask 9 in FIG. 2A) is designed and built for a photolithography process to produce a semiconductor device(s). In step 51, radiation (e.g., 6A and 6B in FIG. 2A) is propagated through the photomask

to produce a feature(s) (e.g., feature 15B in FIG. 2B). In step 53, the feature(s) is measured and to determine if the feature(s) comprises a CD error. Measuring techniques may include, inter alia, using an SEM, etc. If a CD error is not found in the feature in step 53, then in step 61 a semiconductor device manufacturing process may continue to produce a semiconductor device(s). If it is determined in step 53 that due to an error (e.g.,an incorrect pattern or image on a mask, an error during a pattern transfer from the mask to the photoresist, an incorrect original design, etc) the feature(s) comprises a CD error then in step 55, the CD error is analyzed to determine a dose of electron beam exposure that may be used to correct the CD error in a subsequent step. A method for determining the dose of electron beam exposure is described with reference to FIG. 7 as described, infra.

[0051] In step 57, the feature(s) is exposed to the dose of electron beam exposure, thereby shrinking the feature size, and ultimately correcting the CD error (e.g., feature 15C in FIG. 3B) . In step 59, a semiconductor device manufacturing process is completed thereby producing a semiconductor device(s) (e.g., a semiconductor chip) without a CD error(s).

[0052] FIG. 6 is a flowchart depicting an algorithm 65 for a final semiconductor device (e.g., a semiconductor chip) based method for correcting a CD error at a photoresist level, in accordance with embodiments of the present invention. The algorithm 65 is described with reference to FIGS, 2A, 2B, 2C, and 2D. In contrast to the algorithms 22 and 47 of FIGS. 4 and 5, the process of algorithm 65 of FIG. 6 comprises building a first semiconductor device(s) with a CD error(s) and using the first semiconductor device(s) to correct the CD error(s) during a process to build subsequent semiconductor devices.

[0053] In step 67, a photomask (e.g., photomask 9 in FIG. 2A) is designed and built for a photolithography process to produce a semiconductor device(s). In step 69, the photomask of step 67 is used during the photolithography process to produce a first

semiconductor device(s). In step 73, first semiconductor device(s) is characterized to determine a CD error(s). Characterizing the first semiconductor device(s) may comprise performing a functionality test of the first semiconductor device to determine an actual operating speed for the first semiconductor device (e.g., a signal speed between or within various circuits within the semiconductor device, a signal speed within an individual component (transistor, resistor, capacitor, etc)). Alternatively, the characterization may include determination of other physical dimensions, such as current, resistance, or capacitance. Based on a comparison of the actual operating conditions of the first semiconductor device and either a calculated or designed operating characteristic of the first semiconductor device or an actual operating charicteristic of a second semiconductor device known to comprise no CD errors, it may be determined that specific circuits are not operating correctly due to specific electrical components (e.g., transistor, capacitor, resistor) or a combination therein that comprise(s) a CD error(s). If a CD error is not found in step 73, then in step 74 a semiconductor device manufacturing process may continue to produce a semiconductor device(s). If in step 75, a CD error(s) is found, or it is determined that a deliberate CD error may enhance the functionality of the semiconductor device, the CD error(s) is analyzed to determine a dose of electron beam exposure that may be used to correct the CD error in during a photolithography process to build a second semiconductor device(s) using the photomask of step 67. A method for determining the dose of electron beam exposure is described with reference to FIG. 7 as described, infra. In step 77, radiation (e.g., radiation 6A and 6B in FIG. 2A) is propagated through the photomask comprising the CD error thereby producing a feature(s) (e.g., feature 15B in FIG. 2B) comprising the CD error. In step 79, the feature(s) is exposed to the dose of electron beam exposure, thereby shrinking the feature size, and ultimately correcting the CD error (e.g., feature 15C in FIG. 3B).

[0054] In step 83 a semiconductor device manufacturing process is completed thereby producing a semiconductor device(s) (e.g., a semiconductor chip) without a CD error(s).

[0055] FIG. 7 is a graph comprising test data for providing a relationship between a plurality CD size (i.e., dimension) change for a feature(s) and a plurality of electron beam exposures to the feature so that a specific dose of electron beam exposure may be selected based on an amount CD size change required to correct the CD error for a feature(s), in accordance with embodiments of the present invention. The photoresist material used in FIG. 7 is AR237J manufactured by Shipley. Note that any photoresist material may be used thereby producing a different characteristic response to e-beam exposure. The feature comprises a line formed in photoresist. The Y-axis represents a CD size (i.e., dimension) change in nanometers. The X-axis represents a plurality (i.e., 10) exposures of 3 seconds each to a 500eV electron beam. The values for CD size (i.e., dimension) changes with respect to a number exposures of 3 seconds each to a 500 eV electron beam are represented by data points 100-110. As illustrated by the data points 100-110, it may be determined that as the number of electron beam exposures increase, so does the amount of size change for the critical dimension(s). Therefore, using the graph of FIG. 7, a dose of electron beam exposure may be determined for a specific CD error. For example, if a 12 nanometer CD size change is required to correct a CD error, then by viewing data point 104 on the graph of FIG. 7 it may be determined that 12 seconds of exposure (i.e., 4 exposures * 3 seconds per exposure) to the 500eV electron beam (i.e., the dose of electron beam exposure) will correct the CD error (12 nanometers). Thus, three exposures of 4 seconds each, would alternatively cause a 12 nanometer CD size change.

[0056] While embodiments of the present invention have been described herein for purposes of illustration, many modifications and changes will become apparent to

those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the true spirit and scope of this invention.